

# Temperature-Dependent Transfer Characteristics of Amorphous InGaZnO<sub>4</sub> Thin-Film Transistors

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The transfer characteristics of amorphous InGaZnO<sub>4</sub> thin-film transistors (a-IGZO TFTs) were measured at temperatures ranging from 298 to 523 K in order to analyze the behavior of the above-threshold (ON state) and subthreshold regions. For comparison, the transfer characteristics of a hydrogenated amorphous silicon TFT (a-Si:H TFT) were measured in the same temperature range. We developed a simple analytical model that relates the threshold voltage ( $V_t$ ) decrease due to increasing temperature to the formation of point defects in a-IGZO. It is well known that the formation of point defects results in the generation of free carriers in oxide semiconductors. Incorporating the analytical model with the experimental transfer characteristics data taken at high temperatures over 423 K, we estimated the formation energy to be approximately 1.05 eV. The  $V_t$  decrease because of the generation of point defects is peculiar to a-IGZO TFTs, which is not observed in a-Si:H TFTs. The results for the ON-current activation energy suggested that the density of tail states for a-IGZO is much lower than that for a-Si:H. © 2009 The Japan Society of Applied Physics

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## 1. Introduction

Novel thin-film transistor (TFT) devices incorporating transparent amorphous oxide semiconductors are causing the rapid evolution of TFT-based electronics such as flat-panel displays and electronic papers. Hosono, Nomura, Kamiya, and their coworkers pioneered the material science for transparent amorphous oxide semiconductors and have made a considerable impact in the field of TFT technologies with their technological achievement of amorphous InGaZnO<sub>4</sub> (a-IGZO) TFTs.<sup>1–5</sup> Their achievement has been followed by several experimental studies demonstrating the prototypes of flat-panel displays and electronic circuits based on a-IGZO TFT arrays.<sup>6–10</sup> One of the main electrical features of a-IGZO TFTs includes their field-effect mobility being higher than that of the hydrogenated amorphous silicon (a-Si:H) TFTs that are currently utilized in active-matrix liquid-crystal displays. In addition, the device structure and fabrication process are compatible with those of a-Si:H TFTs. Substituting a-Si:H TFTs with a-IGZO TFTs would make it possible to improve the performance of the flat-panel displays because of the transparency as well as the higher field-effect mobility.

In terms of the material and device physics, there still remain some issues peculiar to a-IGZO that have not been fully understood. Differently from a-Si:H, the most distinctive characteristic of a-IGZO is its carrier generation mechanism. At temperatures below room temperature, the dominant mechanism for carrier transport in a-Si:H is ascribed to variable-range hopping, while band conduction occurs easily in a-IGZO.<sup>2,4</sup> In contrast, with respect to the carrier generation and transport at higher temperatures (above room temperature), which are of interest in this article, free carriers in a-Si:H are thermally activated, and thus, band transport, which is sporadically interrupted by trapping at the localized tail states below the conduction-band mobility edge  $E_c$ , contributes to the conductivity. On the other hand, free carriers in a-IGZO mainly originate from point defects in the system. The density of the point defects in a-IGZO, which significantly affects its electrical con-

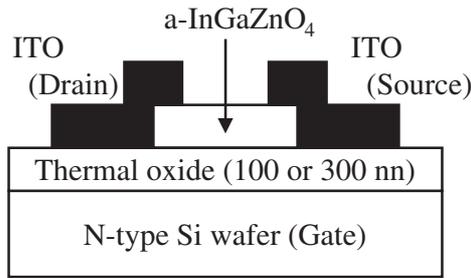
ductivity, will be primarily determined by the method and condition of the film preparation. In addition, there are some other factors that determine the density of point defects. In terms of thermal equilibrium, the ambient temperature will be responsible for the generation of point defects. Such point defects would have a considerable effect on not only the a-IGZO conductivity but the characteristics of a-IGZO TFTs as well. It is therefore important to investigate how the a-IGZO TFT characteristics are sensitive to the ambient temperature that affects the density of point defects in a-IGZO.

In this article, we evaluate the temperature dependence of the electrical characteristics of a-IGZO TFTs, in comparison with those of a-Si:H TFTs. We will discuss the differences in the temperature dependence between the two types of TFTs, with emphasis on the unique behavior for the transfer characteristics of a-IGZO TFTs. We will develop an analytical model that relates the unique behavior with the generation of point defects due to increasing temperature.

## 2. Experiment

We deposited a-IGZO films in an Ar/O<sub>2</sub> gas mixture at room temperature using an rf magnetron sputtering technique. The total gas pressure and the partial pressure of O<sub>2</sub> during the deposition were 0.5 and 0.005 Pa, respectively. We conducted X-ray diffraction (XRD) and thermal desorption spectrometry (TDS) measurements to evaluate the properties of the a-IGZO films. Before the measurements, the a-IGZO films were annealed at 603 K for 1 h. The TDS data were used to evaluate the thermal stability of the a-IGZO films. Weakly bonded or trapped atoms in a-IGZO films will be desorbed with increasing sample temperature, resulting in the desorption peaks for the atoms in the spectra.

Figure 1 shows the cross section of the inverted-staggered bottom-gate a-IGZO TFT used in this study. We fabricated a-IGZO TFTs on the highly doped n-type silicon wafers having a thermal oxide layer (SiO<sub>2</sub>) of 100 or 300 nm. The n-type silicon and thermal oxide act as the gate electrode and gate insulator, respectively. The a-IGZO active layer was deposited under the same condition mentioned above. The



**Fig. 1.** Cross section of the inverted-staggered bottom-gate amorphous InGaZnO<sub>4</sub> TFT structure used in this study.

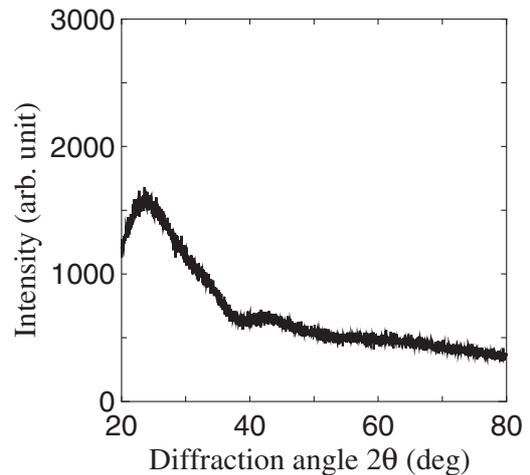
indium–tin oxide (ITO) source/drain electrode layer was deposited in an Ar/O<sub>2</sub> gas mixture at room temperature by dc magnetron sputtering, yielding a  $\sim 10^{-4}$ - $\Omega$  cm material. Such low resistivity of the ITO layer allows us to obtain satisfactory ohmic contacts at the source/drain regions. The thicknesses of the a-IGZO and ITO layers are 20 and 50 nm, respectively. The TFT has a channel length of 50  $\mu$ m and a channel width of 100  $\mu$ m.

The transfer characteristics of a-IGZO TFTs were measured at various temperatures  $T$  (from 298 to 523 K) for the gate voltages  $V_g$  ranging from  $-10$  to  $10$  V with a fixed drain voltage  $V_d = 1$  V. For comparison, we also measured the transfer characteristics under the same condition for an inverted-staggered bottom-gate a-Si:H TFT utilizing silicon nitride (SiN<sub>x</sub>) as the gate insulator.<sup>11)</sup> The thickness of the a-Si:H layer is 30 nm. The structure of the a-Si:H TFT is a back-channel-etched type without an ordinary SiN<sub>x</sub> passivation layer. The temperature-dependent characteristics measurements were conducted with an HP4156C semiconductor parameter analyzer in an atmosphere of dried air. Prior to the measurements, all the TFT samples used in this study were annealed at 603 K for 1 h. This annealing process eliminates any processing damage during the TFT fabrication and brings the TFT samples into a reproducible initial state.

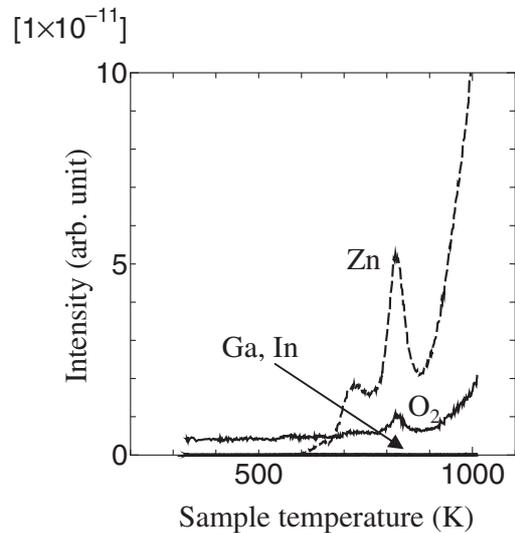
### 3. Results and Discussion

Figure 2 shows an X-ray diffraction pattern for an a-IGZO film deposited on a glass substrate. The halo peak around 25° is due to the glass substrate. No other peaks are observed, indicating that the film is amorphous, which is consistent with the previous observation that the amorphous structure of a-IGZO films is stable up to around 773 K in air.<sup>5)</sup>

Figure 3 shows TDS data for the a-IGZO film annealed at 603 K for 1 h. The desorption spectra of O<sub>2</sub>, Zn, Ga, and In were measured as a function of the sample temperature. The desorption spectra for O<sub>2</sub> and Zn have the peaks at approximately 723 and 823 K and rapidly increase in the temperature range over 900 K. On the other hand, the desorption of Ga and In is negligible in the entire temperature range investigated, suggesting that Ga–O and In–O bondings are more stable than Zn–O bonding. This result is consistent with the fact that Ga ions form stronger chemical bonds with oxygen than Zn ions do.<sup>5)</sup> It is worth noting that a clear desorption is not observed for the four elements in the temperature range from 298 to 523 K used in the TFT measurements. This indicates that, as far as the thermal desorption is concerned, the IGZO film incorporated into the TFTs is stable in this temperature range.



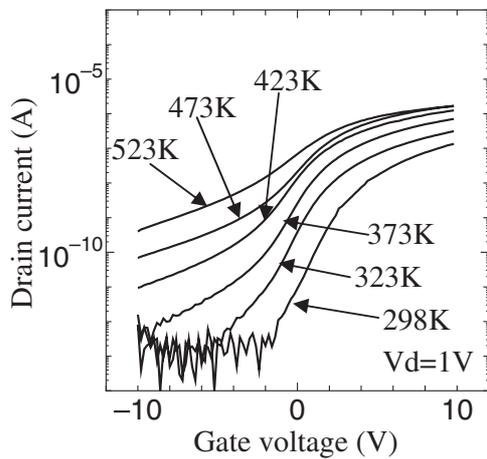
**Fig. 2.** XRD pattern for an a-IGZO film annealed at 603 K for 1 h.



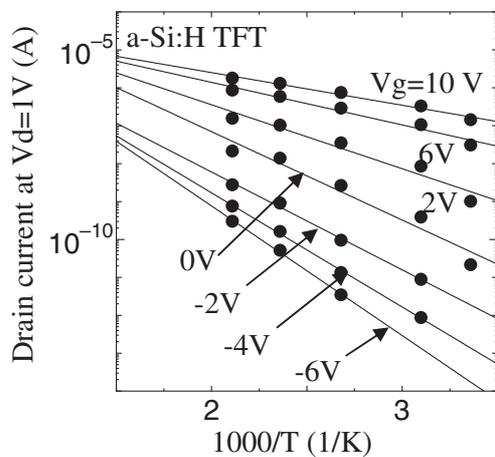
**Fig. 3.** TDS spectra for O<sub>2</sub>, Zn, Ga, and In for the same a-IGZO film as in Fig. 2.

Figure 4 shows the transfer characteristics at different temperatures for the a-Si:H TFT with a 30 nm a-Si:H layer. As seen in this figure, the drain current in the entire  $V_g$  region increases with increasing temperature. The field-effect mobility is approximately  $0.5 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$  at room temperature. Figure 5 shows the Arrhenius plots of  $\ln I_d$  vs  $1000/T$  for different gate voltages, where  $I_d$  denotes the drain current. We clearly see that both the ON current in the above-threshold region and the subthreshold current are thermally activated with the activation energy  $E_a$  that depends on the gate voltage. A similar behavior has been observed for typical a-Si:H TFTs in the temperature range of less than 433 K.<sup>12–17)</sup>

Figures 6(a) and 6(b) show the typical transfer characteristics at different temperatures for a-IGZO TFTs having the SiO<sub>2</sub> gate dielectric layer of (a) 100 and (b) 300 nm, respectively. The field-effect mobility of these TFTs is approximately  $10 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ , which is approximately one order of magnitude higher than that of typical a-Si:H TFTs. There are three distinctive regions in the transfer characteristics, namely, the above-threshold region, subthreshold

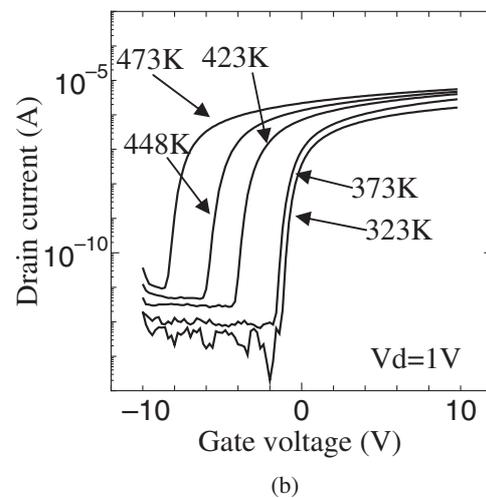
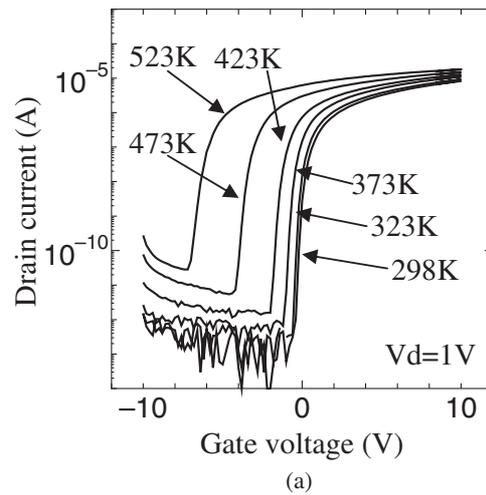


**Fig. 4.** Transfer characteristics at different temperatures for an inverted-staggered bottom-gate a-Si:H TFT.



**Fig. 5.** Arrhenius plots of  $\ln I_d$  vs  $1000/T$  in the subthreshold and above-threshold regions for the a-Si:H TFT.

region, and gate-leakage region. We have confirmed that the gate-leakage current flows through the thermally oxide  $\text{SiO}_2$  gate insulator into the highly doped Si gate electrode. The relatively high gate leakage could be due to the large area of the source/drain electrodes that overlap with the gate electrode (approximately  $1 \text{ mm}^2$ ). In the gate-leakage region, the gate-leakage current seems to be thermally activated. This behavior might be related to the properties of the gate oxide layer and the issue is beyond the scope of this article. Here, we compare the temperature dependence of the transfer characteristics of a-IGZO TFT with those of a-Si:H TFT. The ON current in Fig. 6 seems to be thermally activated, similarly to the case of a-Si:H TFT shown in Fig. 4. It is important to note that, in comparison with the a-Si:H TFT, the behavior of the subthreshold current for the a-IGZO TFT is entirely different. With increasing temperature, the subthreshold current curve is significantly shifted to the negative  $V_g$  direction, which is not observed for the a-Si:H TFT in Fig. 4. It should be noted that the transfer characteristics at room temperature (298 K) were reproducible after the measurements at high temperatures, implying that the change in the transfer characteristics due to increasing temperature is reversible.



**Fig. 6.** Transfer characteristics at different temperatures for a-IGZO TFTs having the  $\text{SiO}_2$  gate dielectric layer of (a) 100 and (b) 300 nm.

In reference to Figs. 6(a) and 6(b), we next discuss the unique behavior of the subthreshold current for a-IGZO TFTs. Here, we expediently define the threshold voltage  $V_t$ , which separates the subthreshold and above-threshold regions, as a gate voltage that gives a drain-current value of  $10^{-7} \text{ A}$ . The lower  $V_t$  observed for the increased temperatures in Fig. 6 may be associated with the generation of point defects, peculiar to oxide semiconductors. It is well known for oxide semiconductors that the free electrons in the materials are mainly due to the generation of oxygen vacancies.<sup>18–20</sup> Thermally excited oxygen atoms that can leave their original sites induce vacancies (point defects) with remaining free electrons at the sites. The excited oxygen atoms that have left their original sites will move into the interstitial sites. The lower  $V_t$  observed at the higher temperatures can be attributed to these free electrons generated along with the oxygen vacancies. We assume that an oxygen vacancy induces two free electrons. According to the statistical thermodynamics, in order to minimize the free energy of the system, it is inevitable that point defects are generated depending on the ambient temperature.<sup>21,22</sup> The generation of point defects increases the internal energy of the system and at the same time increases the entropy of the system, resulting in the minimization of the free energy. In addition, since the defect formation involves the carrier

generation, the charge neutrality needs to be taken into account. On the basis of the assumption that the density of point defects  $n$  is much lower than the densities of lattice and interstitial sites,  $n$  is given as

$$n = C_1 \times \exp\left(-\frac{W}{3k_B T}\right), \quad (1)$$

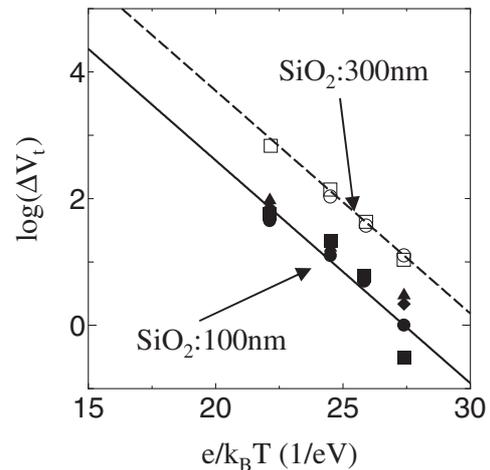
where  $C_1$  denotes the constant related to the entropy for the formation of one vacancy and two free electrons,  $k_B$  the Boltzmann constant, and  $W$  the defect formation energy. The  $V_t$  decrease ( $\Delta V_t$ ) seen in Fig. 6 can be thus related to  $W$  by

$$\begin{aligned} & 2 \times e \times t_{\text{IGZO}} \times C_1 \\ & \times \left[ \exp\left(-\frac{W}{3k_B T}\right) - \exp\left(-\frac{W}{3k_B T_{\text{room}}}\right) \right] \\ & = \Delta V_t \times C_g, \end{aligned} \quad (2)$$

where  $T_{\text{room}}$  stands for the room temperature,  $C_g$  the capacitance of the gate insulator,  $e$  the electronic charge, and  $t_{\text{IGZO}}$  the thickness of the a-IGZO semiconductor layer. Equation (2) is based on the analogy with n-type (donor-doped) silicon materials. It is known for Si-based metal-oxide-semiconductor field-effect transistors (MOSFETs) that the shift of  $V_t$  is closely related to the carrier density per unit area in the bulk silicon. We compare the behavior of Si-based MOSFETs with that of a-IGZO TFTs. We consider that there is an analogy between doping phosphorus into silicon and increasing temperature of a-IGZO in a way that both of them induce free electrons in the semiconductor materials. Thus, we consider that the right-hand side of eq. (2) can be related to the left-hand side representing the change in the bulk carrier density per unit area. In other words, the a-IGZO active layer at high temperatures would act as if it were a highly donor-doped material. Similarly to the accumulation mode of MOSFETs with highly doped silicon, the generation of electrons in a-IGZO at the high temperatures will lead to the significant  $V_t$  decrease. We apply eq. (2) to the data taken at temperatures much higher than room temperature (298 K). If  $W$  is much higher than the energy at room temperature (0.026 eV), then the second term on the left-hand side of eq. (2) can be neglected, which is the case in this study as will be discussed below. Taking the logarithm of both sides of eq. (2) while dropping the second term, we obtain

$$\ln(\Delta V_t) = -\frac{W}{3k_B T} - \ln\left(\frac{C_g}{2 \times e \times t_{\text{IGZO}} \times C_1}\right). \quad (3)$$

By using the experimental data shown in Figs. 6(a) and 6(b),  $W$  and  $C_1$  can be derived from the slope and the intercept of the straight line expressed using eq. (3). Figure 7 shows plots of  $\ln(\Delta V_t)$  vs  $e/k_B T$  in the temperature range of between 423 and 523 K for six different TFTs (four TFTs with a 100 nm  $\text{SiO}_2$  and two TFTs with a 300 nm  $\text{SiO}_2$ ). The closed and open marks represent the data for the 100 nm  $\text{SiO}_2$  TFTs and the 300 nm  $\text{SiO}_2$  TFTs, respectively. The experimental plots give the proximate straight lines with a  $W$  of 1.05 eV and a  $C_1$  of  $1 \times 10^{21} \text{ cm}^{-3}$  (solid line: 100 nm, dashed line: 300 nm). For both  $\text{SiO}_2$  thicknesses, the model expressed using eq. (3) and the experimental data are in good agreement, indicating the validity of the model. By using these values, the defect density at 473 K is estimated to be approximately  $1.9 \times 10^{17} \text{ cm}^{-3}$ . The estimated defect

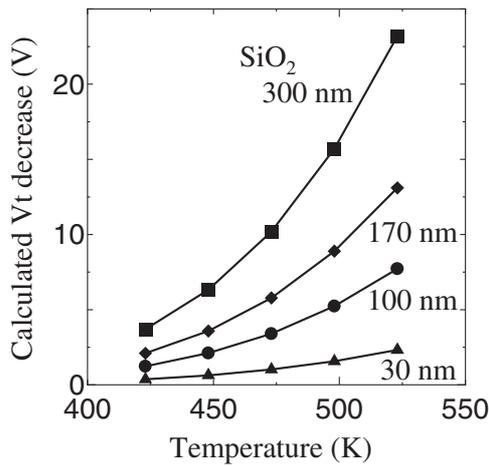


**Fig. 7.** Experimental plots and the proximate straight lines for  $\ln(\Delta V_t)$  vs  $e/k_B T$  in the temperature range of between 423 and 523 K for six different TFT samples (solid line: 100 nm  $\text{SiO}_2$  TFTs; dashed line: 300 nm  $\text{SiO}_2$  TFTs).

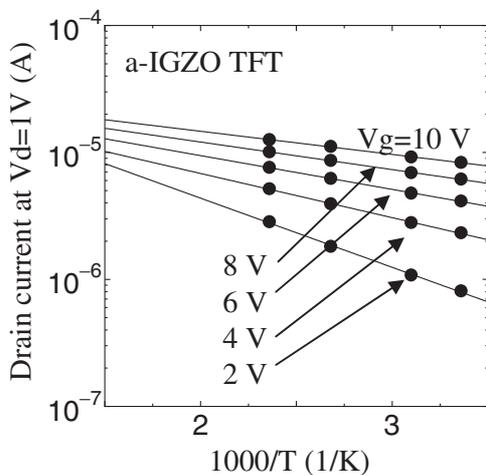
formation energy of 1.05 eV is of the same order as those for typical oxide semiconductor crystals ranging from approximately 0.5 to 2.0 eV.<sup>18,19</sup> As mentioned above, the  $V_t$  decrease due to increasing temperature is reversible, implying that the generated point defects and interstitial oxygen atoms recombine with each other to return to the initial quasi-equilibrium state at room temperature. It is important to add here that the recombination rate would be dependent on the ambient temperature. In this experiment, after the high-temperature measurements, the TFT samples were cooled to room temperature on the heating stage, and thus, the retained heat at the stage is considered to enhance the recombination process. If the TFT samples were instantaneously cooled to room temperature, the recombination process might take more time (a few hours) to reach the initial state.

Since the field-effect mobility values for a-IGZO TFTs are close to those for polycrystalline TFTs, it is possible that self-heating would be a serious issue. Particularly, this would be the case with large-channel-width a-IGZO TFTs that dissipate high electric power. Owing to the self-heating, the temperature of the a-IGZO TFTs would be elevated up to over 420 K, similarly to the case of polycrystalline silicon TFTs.<sup>23–25</sup> From the point of circuit design utilizing a-IGZO TFT arrays, it is important to predict the  $V_t$  decrease at high temperatures for different gate  $\text{SiO}_2$  thicknesses. Using eq. (3) along with the obtained values for  $W$  and  $C_1$ , we calculated the  $V_t$  decrease as a function of the temperature for various  $\text{SiO}_2$  thicknesses. Figure 8 shows the dependence of the calculated  $V_t$  decrease on the temperature for various  $\text{SiO}_2$  thicknesses. As can be seen in this figure, the  $V_t$  decrease significantly changes depending on both the  $\text{SiO}_2$  thickness and the temperature. Therefore, the thickness of the gate insulator should be optimized, taking into consideration the  $V_t$  decrease due to the self-heating.

As stated above, the behavior of the temperature-dependent ON current for a-IGZO TFTs is similar to that for typical a-Si:H TFTs. Figure 9 shows the Arrhenius plots of  $\ln I_d$  vs  $1000/T$  for the a-IGZO TFT in the above-threshold region. The investigated temperature range is below 423 K, where

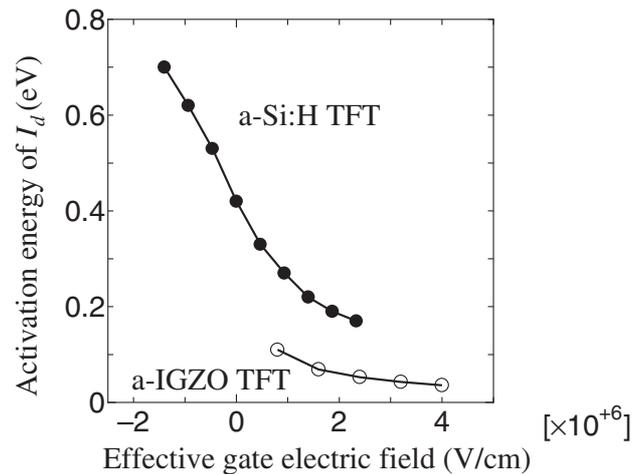


**Fig. 8.** Dependence of the calculated  $V_t$  decrease on the temperature for various  $\text{SiO}_2$  thicknesses.



**Fig. 9.** Arrhenius plots of  $\ln I_d$  vs  $1000/T$  in the above-threshold region for the a-IGZO TFT.

the  $V_t$  decrease due to increasing temperature is very small. The ON current in the above-threshold region seems to be thermally activated. For both a-IGZO TFT and a-Si:H TFT, the dependence of  $E_a$  on the effective gate electric field is summarized in Fig. 10, where the effective gate electric field has been normalized by the thickness and dielectric constant of the gate insulator. It is well known for amorphous-semiconductor TFTs that most of the charge induced by the gate electric field goes into the tail states with a small fraction going into the conduction band, and the Fermi level  $E_f$  moves closer to the edge of the conduction band with increasing gate electric field.<sup>12-16</sup> The ease of the Fermi-level movement is determined by the distribution of the tail states. The increase in  $I_d$  is due to the fraction of the electrons in the conduction band, which are thermally activated with an activation energy. There have been several reports that the tail states have an exponential energy distribution.<sup>12-14,16</sup> The characteristic energy of the exponential variation of the tail states has been estimated to be less than or comparable to  $k_B T$  at room temperature. Therefore, once the Fermi level moves into the tail states, most of the charge is induced into the states above the Fermi level. Hence, the shift of the Fermi level with gate electric



**Fig. 10.** Dependence of the activation energy  $E_a$  for  $I_d$  on the effective gate electric field for the a-IGZO TFT and a-Si:H TFT.

field is significantly smaller than in the subthreshold region. From this point of view, the minimum activation energy, approached at the highest gate electric field, gives a measure of the tail state distribution. As seen in Fig. 10,  $E_a$  (activation energy of  $I_d$ ) decreases monotonically with the effective gate electric field. As the effective gate electric field is increased positively, the Fermi level  $E_f$  moves closer to the conduction-band edge  $E_c$  until it reaches the tail states. Because of the high density of states, the Fermi level is pinned in the tail states, as indicated by the reduced slope of the  $E_a$  vs effective gate electric field curve in this figure.<sup>13,14,16</sup> Comparison of the  $E_a$  values for both TFTs at an effective gate field of 2.5 V/cm in Fig. 10 shows that the  $E_a$  value for the a-IGZO TFT is as low as one-third of that for the a-Si:H TFT, suggesting that the a-IGZO/ $\text{SiO}_2$  interface has a much steeper tail-state distribution than the a-Si:H/ $\text{SiN}_x$  interface. This result might be ascribed to a much steeper tail-state distribution for bulk a-IGZO than that for bulk a-Si:H.<sup>26</sup> Such steeper tail-state distribution would lead to the lower density of states for a-IGZO than that for a-Si:H at the same energy level. Further study will be required to quantitatively estimate the magnitude of the density of the tail states.

#### 4. Conclusions

Temperature-dependent transfer characteristics measurements were conducted for a-IGZO TFTs as compared to a-Si:H TFT. The  $V_t$  decrease due to increasing temperature, which is characteristic of a-IGZO TFTs, can be associated with the formation of point defects in a-IGZO. Incorporating the developed analytical model with the experimental transfer characteristics data taken at the high temperatures over 423 K, we have estimated the formation energy to be approximately 1.05 eV. As has been predicted using the model, the  $V_t$  decrease is a function of both the ambient temperature and the thickness of the gate insulator. Because the self-heating in a-IGZO TFTs would cause the  $V_t$  decrease, the thickness of the gate insulator as well as the TFT geometrical dimension should be properly designed.

The result for the ON-current activation energy has suggested that the tail-state distribution for the a-IGZO/ $\text{SiO}_2$

interface is much steeper than that for the a-Si:H/SiN<sub>x</sub> interface. An additional increase in the induced charge might be divided between the charge going into the conduction band and the charge induced into the tail states farther from the interface. In this sense, this result could also be associated with a much steeper tail-state distribution for bulk a-IGZO than that for bulk a-Si:H.

- 1) H. Hosono, N. Kikuchi, N. Ueda, H. Kawazoe, and K. Shimidzu: *Appl. Phys. Lett.* **67** (1995) 2663.
- 2) H. Hosono: *J. Non-Cryst. Solids* **352** (2006) 851.
- 3) T. Kamiya, S. Aiba, M. Miyakawa, K. Nomura, S. Matsuishi, K. Hayashi, K. Ueda, M. Hirano, and H. Hosono: *Chem. Mater.* **17** (2005) 6311.
- 4) K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono: *Nature (London)* **432** (2004) 488.
- 5) K. Nomura, A. Takagi, T. Kamiya, H. Ohta, M. Hirano, and H. Hosono: *Jpn. J. Appl. Phys.* **45** (2006) 4303.
- 6) H. Yabuta, M. Sano, K. Abe, T. Aiba, T. Den, H. Kumomi, K. Nomura, T. Kamiya, and H. Hosono: *Appl. Phys. Lett.* **89** (2006) 112123.
- 7) M. Ito, M. Kon, T. Okubo, M. Ishizaki, and N. Sekine: Proc. IDW/AD'05, 2005, p. 845.
- 8) K. Abe, H. Kumomi, K. Nomura, T. Kamiya, M. Hirano, and H. Hosono: Proc. IDW'07, 2007, p. 1779.
- 9) R. Hayashi, A. Sato, M. Ofuji, K. Abe, H. Yabuta, M. Sano, H. Kumomi, K. Nomura, T. Kamiya, M. Hirano, and H. Hosono: SID Int. Symp. Dig. Tech. Pap. **39** (2008) 621.
- 10) Jh. Lee, Dh. Kim, Dj. Yang, Sy. Hong, Ks. Yoon, Ps. Hong, Co. Jeong, Hs. Park, S. Y. Kim, S. K. Lim, S. S. Kim, Ks. Son, Ts. Kim, Jy. Kwon, and Sy. Lee: SID Int. Symp. Dig. Tech. Pap. **39** (2008) 625.
- 11) K. Takechi, N. Hirano, H. Hayama, and S. Kaneko: *J. Appl. Phys.* **84** (1998) 3993.
- 12) H. C. Slade, M. S. Shur, S. C. Deane, and M. Hack: Mater. Res. Soc. Symp. Proc. **424** (1997) 91.
- 13) N. Lustig and J. Kanicki: *J. Appl. Phys.* **65** (1989) 3951.
- 14) M. J. Powell: *IEEE Trans. Electron Devices* **36** (1989) 2753.
- 15) C.-y. Chen and J. Kanicki: Mater. Res. Soc. Symp. Proc. **424** (1997) 77.
- 16) M. Shur, C. Hyun, and M. Hack: *J. Appl. Phys.* **59** (1986) 2488.
- 17) K. D. Mackenzie, A. J. Snell, I. French, P. G. LeComber, and W. E. Spear: *Appl. Phys. A* **31** (1983) 87.
- 18) P. Kofstad: *J. Phys. Chem. Solids* **23** (1962) 1571.
- 19) P. Bonasewicz, W. Hirschwald, and G. Neumann: *Phys. Status Solidi A* **97** (1986) 593.
- 20) V. Gavryushin, G. Raciukaitis, D. Juodzbalius, A. Kazlauskas, and V. Kubertavicius: *J. Cryst. Growth* **138** (1994) 924.
- 21) C. Kittel: *Introduction to Solid State Physics* (Wiley, New York, 1976).
- 22) J. Honerkamp: *Statistical Physics* (Spinger, Berlin, 1998).
- 23) S. Inoue, H. Ohshima, and T. Shimoda: *Jpn. J. Appl. Phys.* **41** (2002) 6313.
- 24) Y. Uraoka, K. Kitajima, H. Yano, T. Hatayama, T. Fuyuki, S. Hashimoto, and Y. Morita: Proc. AM-LCD'04, 2004, p. 337.
- 25) K. Takechi, M. Nakata, H. Kanoh, S. Otsuki, and S. Kaneko: *IEEE Trans. Electron Devices* **53** (2006) 251.
- 26) M. Kimura, T. Nakanishi, K. Nomura, T. Kamiya, and H. Hosono: *Appl. Phys. Lett.* **92** (2008) 133512.