

## Collision-Based Computing Using Single-Electron Circuits

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A single-electron (SE) device based on “collision-based computing (CBC)” is proposed for information processing. CBC is an analog computing in which input signals behave like billiard balls, and the goals of moving balls are regarded as output positions. The proposed SE device consists of arrayed SE oscillators with coupling capacitor between each pair. An SE oscillator is a threshold decision device which can be used as a reaction-diffusion (RD) model, a kind of the analog computation model. The RD model can express the various behaviors of an excited wave, e.g., “moving at a constant velocity” and “disappearing due to collision”. These behaviors are also important for CBC. We designed basic SE-CBC circuits and a full adder as an application, and evaluated their operation by Monte-Carlo computer simulation. The results indicate that this circuit is useful for configuring various types of logical circuits. © 2012 The Japan Society of Applied Physics

### 1. Introduction

Information processing devices with high performance are becoming ever more important worldwide. Design and fabrication of the LSI chip serving as the main component in such devices are critical to obtaining high performance. The key to obtaining high performance is to miniaturize the chip components, which means designing and fabricating a metal–oxide–semiconductor field-effect transistor (MOSFET). However, such miniaturization is close to its limit (the nm level) due to the quantum effect resulting from the very short channel length, very thin gate-oxide (insulator), etc. Among the various devices with nanoscale elements proposed for use in next-generation devices, as described in the ITRS roadmap, the single-electron (SE) devices have been attracting attention as a candidate for the next generation one. This device has the tunneling junctions, which permit electrons to pass through due to the tunneling effect and Coulomb blockade phenomenon.<sup>1–3)</sup> This means that an SE device can control an individual electron, which greatly reduces power consumption compared to MOSFETs, which can control only large numbers of electrons. It also means that an SE device circuit can have higher density because the elements can be fabricated in nm scale.

Various useful SE devices have been proposed,<sup>4)</sup> including the SE transistor,<sup>5–9)</sup> the SE pump,<sup>10–13)</sup> the SE charge-coupled device,<sup>14,15)</sup> the SE memory,<sup>16–19)</sup> the SE reaction-diffusion (RD) circuit,<sup>20)</sup> and the majority logic circuit.<sup>21,22)</sup> However, the most appropriate information processing architecture for SE devices is yet undetermined. We have investigated various architectures for SE devices and have shown that an SE oscillator (SEO), which is an SE device, can be used for the RD circuit, which is an analog computation circuit, by arraying several of them two dimensionally.<sup>23)</sup> The RD model can express the various behaviors of an excited wave,<sup>24–26)</sup> e.g., “moving at a constant velocity” and “disappearing due to collision”, and thus be used in wave information processing devices, such as ones for calculating a Voronoi diagram.<sup>23)</sup> We have now proposed an SE device based on the RD model that is targeted at information processing. Since application of conventional Boolean logic circuits, such as conventional digital LSIs, to such a device is difficult due to the

device’s completely different mode of operation, we applied collision-based computing (CBC),<sup>27–29)</sup> an unconventional computing method. Although application of CBC to an LSI device has been proposed,<sup>30)</sup> it turned out to be impractical for MOSFETs. In contrast, the application of CBC to an SE (SE-CBC) device has a potential as a next-generation computing system.

We have designed an SE-CBC circuit and evaluated its operation by computer simulation using the Monte-Carlo method. We also designed and constructed for evaluation a full adder using our SE-CBC circuit and demonstrated that it operated correctly.

### 2. Single-Electron Collision Based Computing Circuits

In this section, we describe the design of our SE-CBC circuit. In particular, we describe CBC, the SEO, which is the main element of the device, and the circuit design.

#### 2.1 Collision based computing

CBC is an unconventional analog computing method based on “billiard ball logic” that emulates the action of the billiard balls on a table. In CBC process, the balls are regarded as signals so that presence or absence of the ball is regarded as binary signals, logical “0” or “1”. Therefore, CBC can operate as binary logic computing partly. It is targeted at logical operation, as illustrated in Fig. 1.<sup>27)</sup> For instance, if there is a ball only at position “Input A” and it is struck at a 45° downward angle, it will roll to position “Output  $A\bar{B}$ ”. If there is a ball only at position “Input B” and it is struck at a 45° upward angle, it will roll to position “Output  $\bar{A}B$ ”. Furthermore, if there is a ball at “Input A” and at “Input B” and each ball is struck as before, they will collide, rebound, and roll to positions “Output AB”. The key point here is that the positions of the logical outputs depend on the inputs. In addition, two properties are needed for correct operation, when there are multiple input signals (balls), 1) these must move at a constant velocity, and 2) they change direction when they collide and rebound. As a result, the position of the output signal differ from that when there is only one input signal.

#### 2.2 Single-electron oscillator

We previously investigated an SEO consisting of a tunneling junction  $C_j$ , a quantum dot (node), a high-ohmic-value resistor  $R$ , and a bias voltage source  $V_d$ , as shown in

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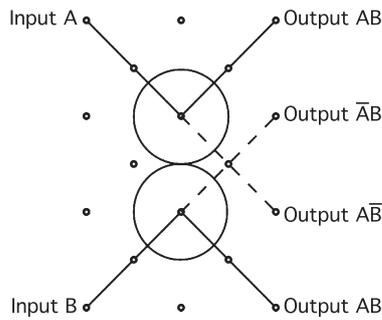


Fig. 1. Schematic illustration of the billiard ball logic.<sup>27)</sup>

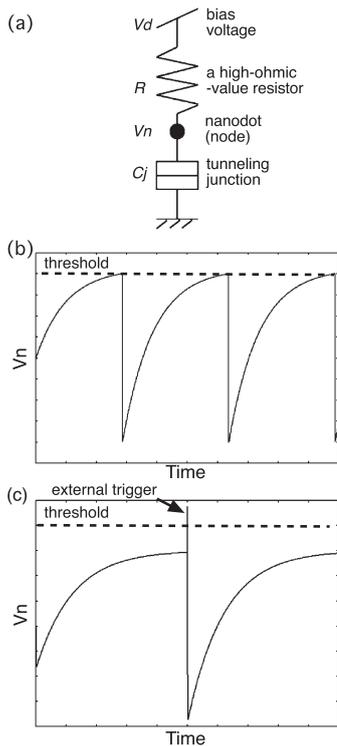


Fig. 2. Single-electron oscillator: (a) circuit configuration, (b) sample node voltage change in “oscillating mode”, and (c) sample node voltage change in “excitatory mode”.

Fig. 2(a). It has a threshold for electron tunneling. When electrons are charged into the node from the bias voltage source, the electrostatic energy of the tunneling junction increases, and the Coulomb blockade effect disappears. The voltage at that moment is the threshold  $V_{th}$ . If the node voltage  $V_n$  exceeds the threshold voltage, an electron tunnels, and the node voltage changes rapidly. The operation of the SEO differs depending on whether bias voltage  $V_d$  is over the threshold voltage. If the bias voltage is over the threshold voltage, there is self-induced oscillation, as shown in Fig. 2(b). This is called “oscillating mode”. On the other hand, if the bias voltage is a little less than the threshold, the node voltage changes only if it receives an external trigger, as shown in Fig. 2(c). This is called “excitatory mode”. The details of this operation are described elsewhere.<sup>20)</sup> We also investigated the operation of arrayed SEOs composing an SE-RD device, as schematically shown in Fig. 3. There are three requirements for arraying the SEOs. First, all the oscillators must be set to excitatory mode. Second, the  $V_d$  of

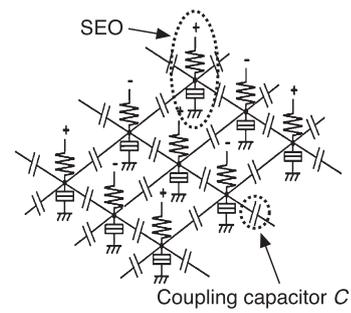


Fig. 3. Circuit configuration of two-dimensionally arrayed SEOs.<sup>20)</sup>

neighboring oscillators must be set to the opposite polarities (+ or -). Third, a coupling capacitor ( $C$ ) must be placed between each pair of SEOs. If these requirements are met, all the SEOs are charged only when there is no signal input. If a signal is inputted to an SEO, an electron tunnels, and the node voltage changes rapidly. This rapid voltage change becomes an input trigger for the neighboring SEOs through the coupling capacitors. In this way, electron tunneling at an SEO induces other tunnelings at the neighbors. This operation causes the excited wave to spread.

With the application of CBC to arrayed SEOs, the spread of the excited wave over the SEOs can be used as a “field” for mimicking the movement of billiard balls moving at a constant velocity. And the direction of the spreading wave can be controlled by changing the connections between SEOs, as described in the next subsection. The “collide and rebound” property can be realized by taking advantage of this feature, as described elsewhere.<sup>20)</sup> Therefore, we can design practical circuits by applying CBC to arrayed SEOs.

### 2.3 Circuit design

The key to designing the SE-CBC circuit is devising a structure for controlling the direction of signal transmission among the arrayed SEOs. Here we describe the special connections we designed for controlling the direction and the SE-CBC circuit we constructed using those connections.

#### 2.3.1 Connections

We designed the three types of connections for the SE-CBC circuit.

The first type is “normal connection”, as schematically shown in Fig. 4(a). The three larger circles represent SEOs, and the “+” and “-” represent the polarity of their bias voltage  $V_d$ . In this type of connection, all bias voltages are set to excitatory mode, and the polarities of the bias voltages of the neighboring SEOs are reversed. The value of  $V_d$  is determined by  $V_{th}$  and  $\Delta V_n$  as shown in Fig. 4(b). Then, the threshold voltage  $V_{th}$  is given by

$$V_{th} = \frac{e + 4C(V_1 + V_2 + V_3 + V_4)}{2(C_j + 4C)}. \quad (1)$$

In this equation,  $V_1$ ,  $V_2$ ,  $V_3$ , and  $V_4$  mean the node voltages of the neighbors. In this connection, there are only two neighbors, so  $V_3$  and  $V_4$  are substituted 0 V. And the change of the SEO node voltage when it receives an input from one of neighbors as a trigger based on the voltage change in it due to the electron tunneling  $\Delta V_n$  is given by

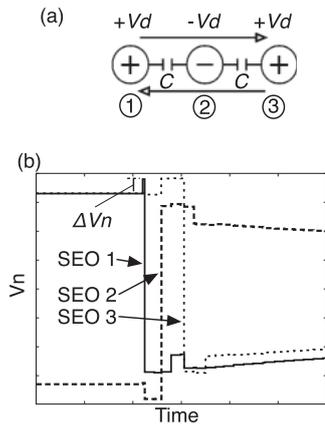


Fig. 4. (a) Schematic diagram and (b) sample node voltage change of each SEO for “normal connection” showing that the signal is transmitted.

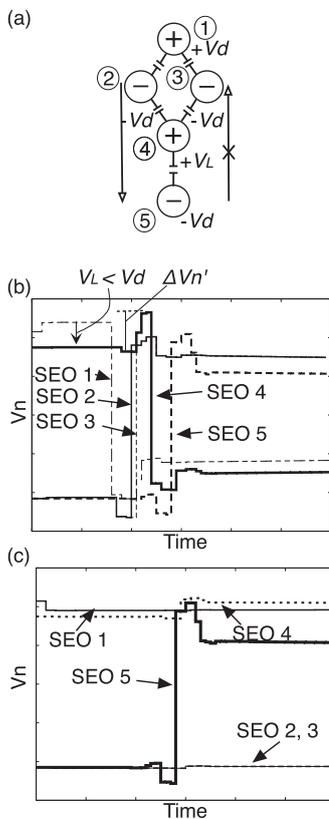


Fig. 5. (a) Schematic diagram and (b, c) sample node voltage change of each SEO for “one-way connection”: (b) signal coming from SEO 1; (c) signal coming from SEO 5. Signal is transmitted as shown in (b), and signal stops at SEO 4, as shown in (c).

$$\Delta V_n = \frac{4CV_1}{C_j + 4C} \tag{2}$$

Then,  $V_d$  is determined according to following condition:

$$V_d < V_{th} < V_d + \Delta V_n. \tag{3}$$

Under these conditions, a signal can be transmitted in either direction, as shown in Fig. 4(b).

The second type is “one-way connection”, as schematically shown in Fig. 5(a). In this type of connection, there are two important points. First, dividing the route of the circuits like from SEO 1 to 2 and to 3. Second, all bias voltages of

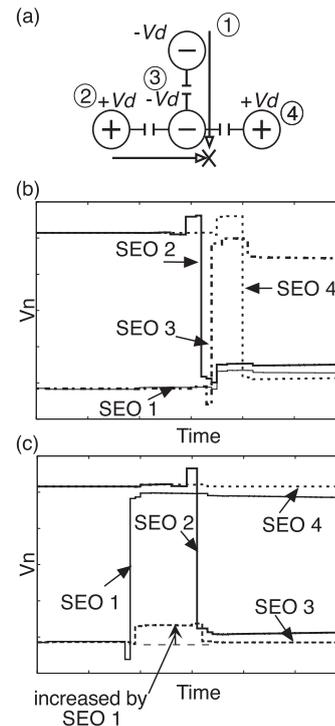


Fig. 6. (a) Schematic diagram and (b, c) sample node voltage change of each SEO for “gate connection”: (b) there is no “block signal” from SEO 1; (c) there is a “block signal” from SEO 1. Signal from SEO 2 is transmitted to SEO 4, as shown in (b), and signal stops at SEO 3, as shown in (c).

the SEOs are set to excitatory mode except for SEO 4. Moreover, bias voltage  $V_L$  for SEO 4 is set slightly less than  $V_d$ . In a  $V_L$ -biased SEO, an electron cannot tunnel if there is only one input and can tunnel if there are two or more inputs.  $V_L$  is determined as follows. Then, the change of the SEO node voltage when the SEO receives two inputs from two of neighbors as a trigger based on the voltage change in it due to the electron tunneling  $\Delta V'_n$  is given by

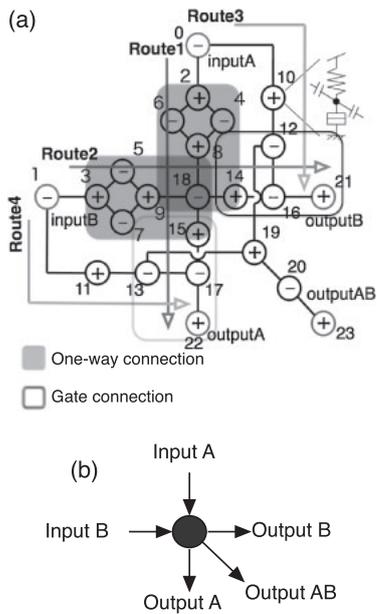
$$\Delta V'_n = \frac{4C(V_1 + V_2)}{C_j + 4C} \tag{4}$$

Then,  $V_L$  is determined according to following condition:

$$V_L + \Delta V_n < V_{th} < V_L + \Delta V'_n. \tag{5}$$

In this condition,  $V_{th}$  and  $\Delta V_n$  can be calculated as with eqs. (1) and (2). Under these conditions, the SEOs of this connection operate in the following manner. When a signal is transmitted from SEO 1, SEO 4 receives the node voltage changes of SEOs 2 and 3, and electron tunneling occurs at SEO 4. When a signal is transmitted from SEO 5, SEO 4 receives only the node voltage change of SEO 5, and electron tunneling does not occur. Figures 5(b) and 5(c) show graphs depicting the node voltage change of each SEO. Thus, a signal can be transmitted in only one direction.

The third type is “gate connection”, as schematically shown in Fig. 6(a). In this type of connection, there is one important point. The polarities between SEOs 1 and 3 are set the same. Under this condition, the SEOs of this connection operate in the following manner. If there is no signal from SEO 1, this connection is a normal connection, so a signal from the left SEO (2) can be transmitted to the right SEO (4), as shown in Fig. 6(b). On the other hand, if there is a signal



**Fig. 7.** Schematic illustration of SE-CBC circuit: (a) diagram; (b) input/output key.

from SEO 1, the node voltage of SEO 3 is increased by the electron tunneling of SEO 1, as shown in Fig. 6(c). Therefore, electron tunneling does not occur at SEO 3 if it receives input from SEO 2. We call this signal from the top a “block signal”, and signaling is stopped if such a signal is received.

### 2.3.2 Constructed circuit

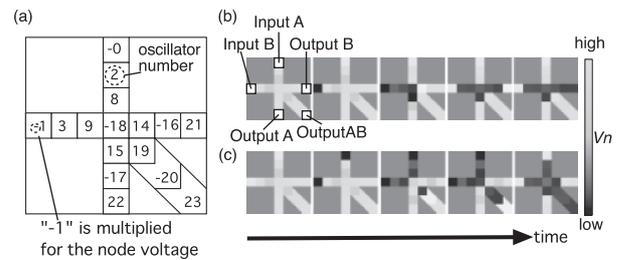
We constructed the SE-CBC circuit schematically illustrated in Fig. 7(a). Figure 7(b) shows the input/output key for the circuit. Several specific operations are needed for this circuit. If the input is to “Input A”, the signal should be output to only “Output A”. If the input is to “Input B”, the signal should be output to only “Output B”. If the input is to both “Input A” and “Input B”, the signal should be output to only “Output AB”. In Fig. 7(a), the shaded areas represent one-way connections, and the rectangular outline areas represent gate connections. For example, if a signal is input to “Input A”, the signal is transmitted along Route 2, and another signal is simultaneously transmitted along Route 4. When the first signal reaches SEO 18, it is not transmitted to SEO 8 because of the one-way connection, and it is not transmitted to SEO 17 because of the gate connection. As a result, the signal is transmitted only to SEO 21.

## 3. Evaluation

We tested the operation of the SE-CBC circuit and of a full adder using this circuit by Monte-Carlo simulation.

### 3.1 SE-CBC circuit

The parameters used to simulate the SE-CBC circuit were  $R = 1.0\text{G}\Omega$ ,  $C_j = 10\text{aF}$ ,  $C = 2.0\text{aF}$ ,  $V_{th} = 4.5\text{mV}$ ,  $V_d = 4.3\text{mV}$ , and  $V_L = 3.5\text{mV}$ .  $V_d$  and  $V_L$  were determined according to §2.3.1. The results were obtained as two-dimensional snapshots of the node voltage at each SEO. The correspondence of the two-dimensional cells to each SEO is shown in Fig. 8(a). The number of cells corresponds to the number of SEOs in Fig. 7(a). The node voltages for SEOs 0,



**Fig. 8.** (a) Relationships between cells of simulation results and number of each SEO shown in Fig. 7(a). (b) Simulation results for SE-CBC circuit for “Input B”; (c) results for “Input A” and “Input B”.

1, 16, 17, 18, and 20 were multiplied by  $-1$  for to facilitate understanding. Figures 8(b) and 8(c) represent the simulation results when the input was to “Input B” and when it was to “Input A” and “Input B”. The bright colored cells represent high voltage, and the dark colored cells represent low voltage. In Fig. 8(b), the cell representing “Input B” turned to dark rapidly comparing first and second from the left snapshot. This means that electron tunneling occurred at the SEO for “Input B”. So we define “0” for the bright colored cells and “1” for the dark colored cells. Given this definition, we can regard that this circuit operates correctly as explained below. When the input is to “Input B”, the cell for “Output B” should turn dark. Conversely, when the input is to “Input A” and “Input B”, the cell for “Output AB” should turn dark. As shown in Fig. 7(a), SEO 19 is not connected directly to SEOs 14 and 15, although the signal seem to jump in Fig. 8(c). The voltage change at SEO 19 is caused by the confluent signals from Routes 3 and 4 of Fig. 7(a). So that the operation of Fig. 8(c) is also correct. Therefore, we could confirm that this circuit operated as mentioned above, so we could evaluate that correct operation.

The results revealed that there was a delay in signal propagation. The propagation delay for the signal to travel from the input point to the output point was about 0.4 ns. It is therefore important to carefully set the timing when the input is to both “Input A” and “Input B”. If there is a non-negligible time lag between “Input A” and “Input B”, the circuit will operate incorrectly. Therefore, the delay should be reduced to ensure correct operation. We call the delay with which the circuit can operate correctly the “acceptable time lag”. In our simulations, the acceptable time lag was about 0.25 ns when the input was to A and B.

### 3.2 Full adder

The full adder we designed for evaluation using the SE-CBC circuit is schematically shown in Fig. 9. The inputs for the upper left circuit were set as “Input A” and “Input B”. The inputs for the upper right and lower left circuits were set as the carry-in signal,  $C_{in}$ . Outputs AB, BC, and CA were set as the carry-out signal,  $C_o (= AB + BC + CA)$ . The sum of outputs A, B, and C were set as signal  $S (= A + B + C)$ . Table I shows the truth table for the full adder. The circuit parameters were set to the same values used for the circuit simulation. “Input  $C_{in}$ ” is inputted 0.4 ns later than “Input A and B” because the propagation delay was about 0.4 ns as shown in previous subsection.

Figures 10(a) and 10(b) respectively show two-dimensional snapshots representing the node voltage of each SEO

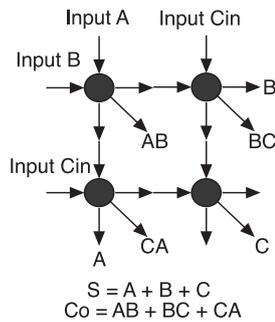


Fig. 9. Full-adder using the SE-CBC circuit.

Table I. Truth table for the full adder.

Input			Output	
A	B	Cin	S	Co
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

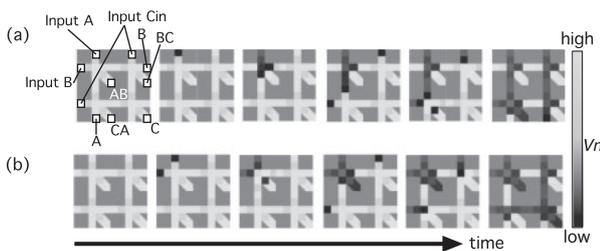


Fig. 10. Simulation results for SE-CBC full adder: (a) Input A and Cin; (b) “Input A” and “Input B” and Cin. (S, Co) = (0, 1) for (a), (S, Co) = (1, 1) for (b).

when the input was to “Input A” and Cin and to “Input A”, “Input B”, and Cin. They show that the adder also operated correctly. Although this adder was not quite a full adder, it could be made into one by simply incorporating two OR logic circuits: the sum signal S operation needs “Output A or B or C”, and the carry-out signal Co operation needs “Output AB or BC or CA”.

#### 4. Discussion

Since the simulation results for the SE-CBC circuit demonstrated that it operated correctly, CBC is suitable for a network of SEOs. Furthermore, we could confirm the acceptable time lag. From the result, we need very careful control which can input to the A and B not to exceed the acceptable time lag. Alternatively, a method could be developed to extend the acceptable time lag. Although the circuit operates incorrectly when the time lag between the two inputs is more than the acceptable time lag, we can make use of this time lag. For example, we could operate the circuit as a parallel information processing device by adjusting the lag. These points remain for future study.

The application of our circuit to a full adder using only four pieces of the SE-CBC circuit and its simulation demonstrated that we can extend and apply the SE-CBC circuit only to array some circuit.

#### 5. Conclusions

We have designed a single-electron collision-based-computing (SE-CBC) circuit for use in an SE oscillator (SEO) as a next-generation computing system. The CBC properties are achieved by controlling the signal direction using three new types of connections: normal, one-way, and gate. We also designed a full adder using the SE-CBC circuit as a demonstration application. Evaluation of their operation using Monte-Carlo computer simulation showed that this circuit can be used to configure various types of logical circuits. We have shown that our SE-CBC circuit can operate as a Boolean logic circuit, and we plan to investigate potential applications of this capability.

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